IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Andreas C. DOERING et al.

Serial No.: To Be Assigned

Filed: Herewith

on both to

Title: METHOD AND APPARATUS FOR USING FPGA TECHNOLOGY WITH A MICROPROCESSOR

FOR RECONFIGURABLE, INSTRUCTION LEVEL HARDWARE ACCELERATION

Mail Stop Patent Application Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT (IDS) UNDER 37 CFR 1.97

Dear Sir:

Applicants submit herewith patents, publications or other information which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 CFR 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

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This Information Disclosure Statement is being submitted with only copies of non-U.S. patent publication(s) and non-patent literature. This protocol conforms with 37 CFR 1.98(a)(2)(i), which waives the requirement for submitting a copy of each cited U.S. Patent and each U.S. patent application publication for all U.S. national patent applications filed after June 30, 2003.

Respectfully submitted,

10 29 03 By:

Stephen G. Sullivan
Sawyer Law Group LLP
Attorney for Applicant(s)

Registration No. 38,329

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	NTS AND PUBLICA INFORMATION STATEMENT	ATIONS FOR	RPS920030110U	JS1	To Be Ass	To Be Assigned		
			APPLICANT:					
			Andreas DOERII	NG et al.				
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)		
	US 2002/0008549	01/24/02	Britton et al.	326	40			
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1	US 2002/0133725	09/19/02	Roy et al.	713	202			
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	US 2003/0025132	02/06/03	Tobey	257	202			
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		FOREIGN PA	ATENT DOCUME	NTS		:		
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLAS	Translation		
•	OTHER ART (In	ncluding Auth	or, Title, Date, P	ertinent Pa	ges, etc.)			
	Microprocessor, F March 2003, pp. 5	PGA, and Custo 21-529.	igurable System Fea omizable I/O," IEEE	Journal of So	olid-State Circui	ts, Vol. 38, No. 3,		
•	Hauser, John R. e	t al., "Garp: A M	IIPS Processor with	a Reconfigu	rable Coprocess	sor," IEEE 1997, pp.		
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		5	9	3	7	1	7	9	08/10/99	Swoboda	395	500		
		6	0	4	1	1	4	0	03/21/00	Binns et al.	382	209		
		6	4	6	7	0	0	9	10/15/02	Winegarden et al.	710	305		
		6	5	0	4	3	9	8	01/07/03	Lien et al.	326	41		
		6	5	0	4	3	9	9	01/07/03	Pani et al.	326	41		
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